REMARKS

Claims 1-5 and 7-12 are presented for examination. The Examiner has withdrawn the rejections of claims 1-5 raised in the previous Office Action.

REJECTION OF CLAIMS 1-5

Claims 1-5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Toshishige in view of Rosenthal et al.

This rejection is respectfully traversed for the following reasons.

Claim 1 recites an apparatus for testing a semiconductor integrated circuit. The testing apparatus comprises:

- a test circuit board constructed so as to exchange a signal with a semiconductor integrated circuit under test; and

- a test ancillary device disposed in the vicinity of the test circuit board.

The semiconductor integrated circuit includes an analog-to-digital converter circuit for converting an analog signal to a digital signal or a digital-to-analog converter circuit for converting a digital signal to an analog signal.

The test ancillary device includes:

- data memory for storing digital test data output from the analog-to-digital converter circuit or digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal, and

- an analysis section for analyzing the digital test data stored in the data memory.

The data memory is divided into two memory sections such that, when digital test data is stored in one memory section, digital test data previously stored in the other memory section is loaded for analysis purposes.

The Examiner takes the position that Toshishige expressly teaches an apparatus containing test circuit board (1), and test ancillary device (8, 6, 9, 11, 13 and 10) disposed in the vicinity of the test circuit board, and having data memory (11) and analysis section (10).

Considering the reference, Toshishige discloses tester 1 that tests device 2. The testing result is transferred to RAM 11 accessed by CPU 10 of the tester 1.

FIGS. 1 and 2 of the reference show that the CPU 10 (considered by the Examiner to correspond to the analysis section of the test ancillary device) is provided in the tester 1. Accordingly, Toshishige does not disclose the test ancillary device having a data memory and an analysis section.

Moreover, the reference discloses a tester rather than a test circuit board, as claim 1 requires.

The Examiner admits that Toshishige does not disclose that the data memory is divided into two memory sections such that, when digital test data is stored in one memory section, digital test data previously stored in the other memory section is loaded for analysis purpose. Rosenthal is relied upon for disclosing this arrangement.

However, Rosenthal discloses a tester having a data processing arrangement. This reference does not disclose the data memory arranged in the test ancillary device, which is disposed in the vicinity of the test circuit board, as claim 1 requires.

Also, Rosenthal does not disclose the data memory for storing digital test data output from the analog-to-digital converter circuit of the semiconductor integrated circuit under test, or digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal

Accordingly, the combined teachings of Toshishige and Rosenthal are not sufficient to suggest a test circuit board and a test ancillary device disposed in the vicinity of the test circuit board and having a data memory for storing digital test data output from the analog-to-digital converter circuit or digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal, and an analysis section, as claim 1 requires.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of *prima facie* obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

As demonstrated above, the combined teachings of the references are not sufficient to arrive at the claimed invention.

Moreover, in rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to provide a reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. ***Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.***, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985). ***In re Fine***, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***Stratoflex, Inc. v. Aeroquip Corp.***, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); ***In re Warner***, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

The Examiner contends that it would have been obvious to incorporate the teaching of Rosenthal into Toshishige's apparatus to provide Toshishige's memory 11 with two memory sections.

However, as discussed above, Toshishige does not disclose the test ancillary device including data memory and an analysis section for analyzing the digital test data stored in the data memory. Accordingly, one skilled in the art would have no motivation to divide Toshishige's memory 11 into two memory sections such that, when digital test data is stored in one memory section, digital test data previously stored in the other memory section is loaded for analysis purpose.

Moreover, Toshishige discloses that all testing data converted by the A/D converter 6 are stored in the RAM 11 at a specific address provided to the CPU 10. When all data are converted, the tester reads them. Therefore, one skilled in the art would have no motivation to divide the RAM 11 into two sections because such a modification would make it more difficult to provide addressing during a testing procedure.

Accordingly, the Examiner has failed to provide the requisite reasons for modifying Toshishige and thus to establish a *prima facie* case of obviousness.

As demonstrated above, the Examiner's conclusion of obviousness in connection with the subject matter of claim 1 is not warranted. Claims 2-5 dependent from claim 1 are defined over the prior art at least for the reasons presented above in connection with claim 1.

Hence, the rejection of claims 1-5 under 35 U.S.C. 103 is improper and should be withdrawn.

REJECTIONS OF CLAIMS 7-12

Claims 7 and 10-12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Toshishige in view of Rosenthal et al. Claims 8-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Toshishige in view of Rosenthal et al. and further in view of Coggins et al.

Independent claim 7 recites a method of testing a semiconductor integrated circuit, which includes at least one of an analog-to-digital converter circuit for converting an analog signal to a digital signal and a digital-to-analog converter circuit for converting a digital signal to an analog signal.

The method uses a test circuit board configured to exchange one or more signals with the semiconductor integrated circuit and a test ancillary device coupled to the test circuit board and including a memory having a first and second sections.

The method comprises the step of storing first digital test data derived from the semiconductor integrated circuit in the first memory section while providing second digital test data derived from the semiconductor integrated circuit and data previously stored in the second memory section to an analysis device configured to analyze digital test data stored in the data memory.

The first and second digital test data are one of an output from the analog-to-digital converter circuit or digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal.

The Examiner takes the position that Toshishige expressly teaches the claimed test circuit board configured to exchange one or more signals with the semiconductor integrated circuit, and the claimed test ancillary device coupled to the test circuit board and including a

memory having a first and second sections.

However, as discussed above, Toshishige does not disclose these claimed elements.

Further, the Examiner contends that Toshishige expressly teaches the step of storing first digital test data derived from the semiconductor integrated circuit while providing second digital test data derived from the semiconductor integrated circuit and data previously stored in the memory to an analysis device configured to analyze digital test data stored in the data memory.

However, as discussed above, Toshishige discloses that the RAM 11 accessible by the tester's CPU 10 stores testing results. Therefore, the reference provides no reason to conclude that this memory stores first digital test data derived from the semiconductor integrated circuit while providing data previously stored in a separate section to an analysis device.

Moreover, the Examiner admits that Toshishige does not disclose storing the first digital data in the first memory section and data previously stored in second memory section. It appears that Rosenthal is relied upon for disclosing this feature.

However, a combination of Toshishige with Rosenthal would not teach or suggest storing first digital test data derived from the semiconductor integrated circuit in a first memory section of a test ancillary device coupled to a test circuit board, while providing data previously stored in the second memory section of the test ancillary device to an analysis device.

Accordingly, the combined teachings of the references are not sufficient to arrive at the claimed invention.

Moreover, as discussed above, the Examiner has failed to provide the requisite reasons for modifying Toshishige and thus to establish a *prima facie* case of obviousness.

Claims 8-12 dependent from claim 7 are defined over the prior art at least for the reasons presented above in connection with claim 7.

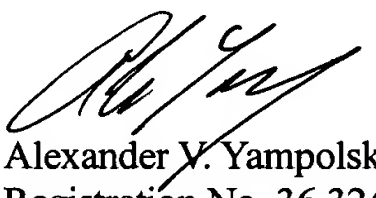
Therefore, the rejection of claims 7-12 under 35 U.S.C. § 103 is not warranted and should be withdrawn.

In view of the foregoing, and in summary, claims 1-5 and 7-12 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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